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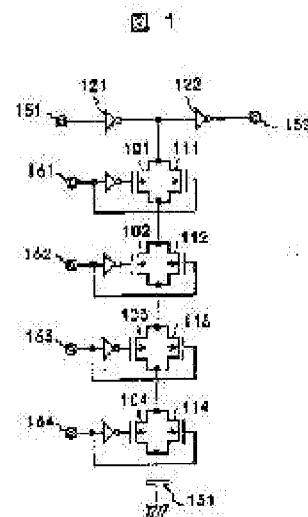
(72)Inventor : MASUDA NOBORU
YAMAMOTO KAZUMICHI
NAKAJIMA KAZUNORI
OKABE TOSHIHIRO
YAMAGIWA AKIRA
YAMAGISHI MIKIO
KOIDE KAZUO
FUJITA BUNICHI
KAWASHIMA SEIICHI

(54) VARIABLE DELAY CIRCUIT

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a clock phase adjustment device that can adjust the phase with high accuracy for a circuit with a greater delay time dispersion in components such as a MOS LSI and even under an environment where temperature fluctuations are greater and to provide a variable delay circuit for the clock phase adjustment device.

SOLUTION: The variable delay circuit is configured with transfer gates 101 to 104 and 111 to 114 that select the magnitude of loads. Further, for the variable delay circuit where a selector circuit selects a path with a different delay time, when a path with a short delay time is selected, a path bypassing part of the selector circuit is provided. The above variable delay circuits of two kinds above are employed so as to make the former variable delay circuit follow a temperature change and the latter variable delay circuit adjust a phase difference due to component dispersion. Thus, it is not especially required to provide a high-speed circuit to follow a temperature change during operation and a minimum delay time of the variable delay circuit can be shortened. Thus, the delay time dispersion in the variable delay circuit itself can easily be reduced.



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CLAIMS

[Claim(s)]

[Claim 1]When it has the following and the above-mentioned transfer gate circuit controls the number of transfer gates of switch-on including two or more transfer gates by which the series connection was carried out, A variable delay circuit controlling switch-on of the above-mentioned transfer gate circuit, and controlling propagation delay time during input and output.

An input terminal.

A buffer circuit which receives a signal inputted from this input terminal.

A transfer gate circuit connected to an output of this buffer circuit.

An output terminal which outputs a signal from an output of the above-mentioned buffer circuit, and a node of a transfer gate circuit.

[Claim 2]The variable delay circuit according to claim 1 the above-mentioned transfer gate circuit's carrying out multiple connection of the transfer gate group which consists of two or more transfer gates by which the series connection was carried out, constituting it, controlling the number of transfer gates of switch-on, and controlling the above-mentioned propagation delay time.

[Claim 3]The variable delay circuit according to claim 2 having at least one inverter circuit between the above-mentioned transfer gate groups.

[Claim 4]PMOS elements to which a control signal is inputted into the above-mentioned transfer gate at a gate, It is a variable delay circuit given in either among claims 1-3 comprising an NMOS element into which the above-mentioned PMOS elements, source, and a drain are connected to in common, and a polar control signal opposite to the above-mentioned control signal to a gate is inputted.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention]Especially this invention relates to the mechanism in which adjust the phase of a clock signal and phase dispersion (skew) is reduced, and the variable delay circuit for it, about the clock signal supply system of information processors, such as a computer.

[0002]

[Description of the Prior Art]As a conventional clock signal feed unit, for example so that it may be indicated by JP,63-231516,A, JP,63-305611,A, or JP,2-168308,A, A clock signal and a reference signal are supplied to two or more distribution destinations from a clock generation part, and what was constituted so that the phase of the clock signal which went via the variable delay circuit for every distribution destination might be doubled with the phase of a reference signal is known. In order to acquire a clock signal with high phase precision with these clock signal feed units, it becomes the point how a reference signal with high phase precision is supplied and how a high-precision phase comparison is performed. In each of above-mentioned articles, various things are indicated about a circuit, a method, etc. of carrying out the circuit and method, and phase comparison which supply the reference signal for it.

[0003]

[Problem(s) to be Solved by the Invention]Although the clock signal of an exact phase is acquired immediately after completing phase adjustment in the phase adjustment device in the conventional clock signal feed unit, if the temperature of a device changes after that, the phase of a clock signal will also change. Therefore, unless it is the narrow systems (namely, expensive system provided with the water cooler etc.) of the temperature change range in a stationary state, if a certain means to follow a temperature change and to control a time delay cannot be found, phase precision will worsen. For example, although an example of the variable delay circuit which can follow a temperature change is shown in JP,2-168308,A, If it is going to make large the range which can be followed without making coarse the resolution (difference of a time delay when a certain control signal is added, and a time delay when only one step changes the control signal) of time delay control, In this circuit, the number of stages of a selector increases and minimum delay time (time delay when the control signal that the time delay of a variable delay circuit becomes the minimum is added) increases. Then, in order that the width of the phase change to the same temperature change may become large and may amend this, the still wider flattery range is needed. Therefore, when making a temperature change follow using the art indicated by JP,2-168308,A, the resolution of phase control had to be made to some extent coarse. This is the 1st technical problem.

[0004]In order to make it not make the clock signal of an output produce a spike shape noise, the timing of the change of a selector is kept from lapping with the standup of a clock signal, or falling in the art indicated by JP,2-168308,A using a flip-flop. However, the high-speed circuit which can follow the frequency of a clock signal is required of such a flip-flop. This is the 2nd technical problem.

[0005]In the variable delay circuit currently used for the conventional clock phase adjusting device, if variable width of a variable delay circuit is enlarged, many number of stageses of a selector will be needed, and minimum delay time will increase. In order that the skew resulting from the manufacturing variation of the semiconductor device which constitutes this variable delay circuit may also become large and may amend this, still bigger variable width is needed. Especially in the CMOS circuit often used for a cheap system, since time delay variation is large, this problem becomes remarkable. This is the 3rd technical problem.

[0006]There is the purpose of this invention in providing the clock signal feed unit which can solve these technical problems and can supply a stable clock signal easily.

[0007]

[Means for Solving the Problem] Solve the 1st and 2nd technical problems of the above, and a variable delay circuit by this invention to achieve the above objects, An input terminal and a buffer circuit which receives a signal inputted from this input terminal, It is characterized by having a transfer gate circuit connected to an output of this buffer circuit, and an output terminal which outputs a signal from an output of a buffer circuit, and a node of a transfer gate circuit, controlling switch-on of a transfer gate circuit, and controlling propagation delay time during input and output.

[0008] A variable delay circuit solve the 3rd technical problem of the above and according to this invention to achieve the above objects, By choosing one from several courses in which time delays differ, respectively, in a variable delay circuit which controls and outputs transfer time of an input signal, the above-mentioned course includes the 2nd controllable course for the 1st course with a constant time delay, and a time delay, and it is characterized by things.

[0009] A clock signal generating part in which the above-mentioned purpose generates a reference signal for phase adjustment of the 1st clock signal and this 1st clock signal using these variable delay circuits, A phase adjustment means which receives the 1st clock signal and reference signal from a clock signal generating part, and generates the 2nd clock signal based on the 1st clock signal and reference signal, In a clock signal feed unit which consists of two or more clock supply destination blocks which it had, respectively, a functional circuit which operates in response to the 2nd clock signal a phase adjustment means, A variable delay means which carries out the series connection of the 1st and 2nd variable delay circuits, is constituted, inputs the 1st clock signal, and outputs the 2nd clock signal, A phase comparison circuit which compares a phase of a reference signal and the 2nd clock signal, and outputs this comparison result, Have a control circuit which controls a variable delay means based on a sequence signal sent from an output and a clock signal generating part from a phase comparison circuit, and a control circuit, The 1st variable delay circuit is controlled at the time of initial adjustment, and it is attained by clock signal feed unit constituting so that the 2nd variable delay circuit may be controlled at the time of operation of a functional circuit.

[0010] By controlling switch-on of a transfer gate connected to an output of a buffer circuit, and changing load of a buffer circuit, resolution of time delay control can be made fine, without enlarging minimum delay time. A time delay can be controlled without changing a course of a clock signal, and generating of a spike shape noise generated with a change of a time delay can be lost.

[0011] The number of a time delay preset value can be made to increase, when a time delay chosen and outputs a signal which passed through a fixed course, and a signal which passed a time delay through a course in which variable is possible, without increasing minimum delay time.

[0012] By performing phase adjustment of a clock signal combining such a variable delay circuit, phase precision is high and a clock signal feed unit which can supply a stable clock signal can be obtained.

[0013]

[Embodiment of the Invention] The 1st example of the variable delay circuit by this invention is shown in drawing 1. The MOS device of the P type which uses 101-104 as a transfer gate in drawing 1, A buffer circuit for 111-114 not to tell the MOS device of the N type used as a transfer gate and the influence of the waveform distortion according [121,122] to a load change to other circuits and 131 are capacitive elements which constitute a part of load. It is a control terminal into which 151 inputs the input terminal of a clock signal into, 152 inputs the output terminal of a clock signal into, and 161-164 input a control signal. If this circuit makes high level all the control signals added to the control terminals 161-164, all the transfer gates will be in switch-on, the load of the buffer circuit 121 will become the heaviest, and the signal propagation time to the output terminal 152 will become the maximum from the input terminal 151. Here, if only the control signal currently added to the control terminal 164 is made into a low level, only the transfer gates 104 and 114 will be in a cut off state, and the load of the buffer circuit 121 will become light only the gate capacitance by the side of the drain of MOS device 104,114, and the part of the capacitive element 131. Therefore, the signal propagation time from the input terminal 151 to the output terminal 152 becomes short only the part. If the control signal currently added to the control terminal 163 is made into a low level, The transfer gates 103 and 113 will be in a cut off state, and, as for the load of the buffer circuit 121, the part of the gate capacitance by the side of the drain of MOS device 103,113 becomes still lighter the sauce [besides the above] side of MOS device 104,114. Therefore, the signal propagation time from the input terminal 151 to the output terminal 152 becomes still shorter [the part]. When similarly the control signal currently added to the control terminal 161 is made into a low level, the propagation time from the input terminal 151 to the output terminal 152 becomes the shortest. Here, the propagation time at that time is not concerned with the number of stages of a transfer gate, but is decided only by the basic delay time of the buffer circuit 121,122, and gate capacitance of load driving capability and MOS device

101,111. That is, if the circuit of drawing 1 is used, it can design to make the resolution of time delay control fine, without increasing minimum delay time. Since the circuit which changes the propagation path of a clock signal itself is not used for the circuit of drawing 1 like the variable delay circuit used conventionally, Unless the control signal added to the gate of the transfer gates 101-114 is changed extremely steeply, there is no possibility that a spike shape noise may arise. Therefore, the buffer circuit 121,122 which a clock signal spreads, and the control circuit which operates at high speed than comparable do not have necessity.

[0014]The 2nd example of the variable delay circuit by this invention is shown in drawing 2. The MOS device of the P type which uses 101-108 as a transfer gate in drawing 2, A buffer circuit for 111-118 not to tell the MOS device of the N type used as a transfer gate and the influence of the waveform distortion according [121,122] to a load change to other circuits and 131,132 are capacitive elements which constitute a part of load. It is a control terminal into which 151 inputs the input terminal of a clock signal into, 152 inputs the output terminal of a clock signal into, and 161-168 input a control signal. The circuit shown in drawing 2 is what provided in parallel the transfer gate of the circuit shown in drawing 1, like the circuit of drawing 1, changes the weight of load and controls a time delay by opening and closing of a transfer gate. When the number of stages of a transfer gate is increased to some extent above, the series resistance of a transfer gate becomes large and load far from the buffer circuit 121 stops contributing to the change of a time delay not much in the circuit of drawing 1. In this example, such a problem is avoided by making a transfer gate parallel.

[0015]The 3rd example of the variable delay circuit by this invention is shown in drawing 3. The MOS device of the P type which uses 101-108 as a transfer gate in drawing 3, The MOS device of the N type which uses 111-118 as a transfer gate, A buffer circuit for 121,122 not to tell the influence of the waveform distortion by a load change to other circuits, a buffer circuit for 123 to avoid reduction of the signal amplitude in this variable delay circuit, and 131,132 are capacitive elements which constitute a part of load. It is a control terminal into which 151 inputs the input terminal of a clock signal into, 152 inputs the output terminal of a clock signal into, and 161-168 input a control signal. If the variable range of a time delay is made or more [of the cycle of a clock signal] into about 1/4, the output swing of the buffer circuit 121 will begin to decrease, and when about 1/2 or more is used, a signal stops getting across to the buffer circuit 122 in the circuit of drawing 1 or drawing 2. In order to avoid such a problem, in this example, the buffer circuit 123 has separated order. For example, by making variable width of the time delay between the buffer circuits 121-123 and between the buffer circuits 123-122 into every [of the cycle of a clock signal / 4 / 1/], respectively, Variable width of the time delay in the whole can be set to 1/2 of the cycle of a clock signal, without decreasing the signal amplitude in a circuit greatly. Since the load driving capability of the buffer circuit 121 generally falls with the time of the standup of a signal and differs by the time, If load is made heavy in the circuit of the 1st and 2nd examples and the circuit of this example will be used to changing while the duty of a clock signal spreads from an input to an output, It is effective in change of duty being amended by making almost equivalent weight of the load before and behind the buffer circuit 123.

[0016]Drawing 4 shows the 4th example of the variable delay circuit by this invention, and combines the circuit of drawing 2, and the circuit of drawing 3. That is, the buffer circuit 123 is formed among the buffer circuits 121 and 122, and it has composition which added further what connected two or more transfer gates to each in series as load of the buffer circuits 121 and 123 to two or more set parallel. As shown in drawing 4, the MOS device which connected the source electrode and the drain electrode to the power supply constitutes the capacitive element 131 from this example. A variable delay circuit with still bigger variable width can also be obtained by [which prepare two or more variable delay circuits as shown in drawing 1 - drawing 4, and has them in how many steps] dropping off.

[0017]The 5th example of the variable delay circuit by this invention is shown in drawing 5. In drawing 5, it is an inverter circuit for 501-508 to double a selector circuit and for 521-529 double the polarity of a clock signal. It is a control terminal into which 551 inputs the input terminal of a clock signal into, 552 inputs the output terminal of a clock signal into, and 561-568 input a control signal. If the control signal that all the selector circuits choose the input (it is the node 511 when it is the selector circuit 501) of the figure bottom is inputted into the control terminals 561-568 in this example, The clock signal inputted into the input terminal 551 is outputted to the output terminal 552 via all the inverter circuit and all the selector circuits. This state is in the state set as the maximum delay time of this circuit. If the control signal inputted into the control terminal 568 here is changed, the selector circuit 508 will come to choose the signal from the inverter circuit 527, and the signal which does not go via the inverter circuit 528,529 will be outputted. Therefore, signal propagation time becomes short by the time delay of the inverter circuit

528,529. If the control signal inputted into the control terminal 567 is changed, the selector circuit 507 will come to choose the signal from the inverter circuit 526, and the signal which does not go via the inverter circuit 527 and the selector circuit 508 further, either will be outputted. Therefore, only the part becomes short further about signal propagation time. When similarly the control signal inputted into the control terminal 561 is changed, the signal which does not go via any circuits other than selector circuit 501 at all will be outputted. The signal propagation time from the input terminal 151 at this time to the output terminal 152 is not concerned with the number of the selector circuits in the whole, but is decided only by the time delay of the selector circuit 501, and becomes the shortest. That is, according to this example, maximum delay time can be designed arbitrarily, without increasing minimum delay time.

[0018]Drawing 6 shows an example of the selector circuit 501 which is a component of the delay circuit of drawing 5. As for 601–604, in drawing 6, the MOS device of N type and 621 are inverter circuits the MOS device of P type, and 611–614. The control terminal into which 551 inputs the input terminal of a clock signal into, 552 inputs the output terminal of a clock signal into, and 561 inputs a control signal, the terminal which connects 511 to the output of the selector circuit 502 in drawing 5, and Vdd are the terminals linked to the power supply of straight polarity. If this circuit adds the control signal of a low level to the control terminal 561, PMOS elements 604 and the NMOS element 613 will be in a cut off state, and PMOS elements 603 and the NMOS element 614 will be in switch-on. Therefore, the signal which appears in the output terminal 552 will be decided by the state of PMOS elements 602 and the NMOS element 612. That is, what reversed the signal added to the input terminal 551 will appear in the output terminal 552, and the influence of the signal added to the input terminal 511 does not win popularity. On the contrary, if a high-level control signal is added to the control terminal 561, PMOS elements 603 and the NMOS element 614 will be in a cut off state, and PMOS elements 604 and the NMOS element 613 will be in switch-on. In this case, what reversed the signal added to the input terminal 511 will appear in the output terminal 552, and the influence of the signal added to the input terminal 551 does not win popularity. Thus, the circuit 501 shown in drawing 6 operates as a selector circuit. Other selector circuits 502–508 in drawing 5 can be constituted similarly. What is necessary is just to use a selector circuit as shown, for example in drawing 23 of JP,2–168308,A, in sending a clock signal by differential. Since it can set up freely [polar being reversal or being un-reversed] only with a connection method when sending a clock signal by differential, it is obvious that the inverter circuits 521–528 of drawing 5 become unnecessary.

[0019]One example of the control circuit which generates the control signal to the variable delay circuit of the 1st explained above – the 5th example is shown in drawing 7.

[0020]In drawing 7, 901–906 are flip-flop circuits. The output terminal of the control signal which 961–966 give to a variable delay circuit, The terminal which inputs a DOWN signal for the terminal which inputs a UP signal for 971 to make a time delay increase, and 981 to decrease a time delay, and 991 are terminals which input the clock signal of a low frequency wave in order to operate this circuit. All the signals with which this circuit appears in the internal nodes 972–976, and 982–986 when the signal of a low level is added to the terminals 971 and 981 serve as a low level. Then, the signal added to the input of the flip-flop circuits 901–906 becomes the same thing as the signal which has appeared in the terminal of 961–966, respectively, and even if a clock signal is added to the terminal 991, the state of all the flip-flop circuits is held as it is. Next, the case where a high-level signal is added to the terminal 971 making the terminal 981 into a low level is considered. Here, it is assumed that high level appears in the output terminals 961–963, and a low level has appeared in the output terminal 964 temporarily for example. At this time, it is set to the signal which appears in the internal nodes 972–974 being high-level, and the signal which appears in the internal node 975,976 serves as a low level. If a clock signal is added to the terminal 991 in this state, the signal which appears in the output terminal 964 will change from a low level high-level, and the output terminals 961–963 will become high-level with as. The signal which appears in the output terminals 965–966 is held as it is. That is, if a high-level signal is added to the terminal 971, making the terminal 981 into a low level, whenever a clock signal will be added to the terminal 991, only the terminal of a low level which is most in right-hand side in the output terminals 961–966 changes high-level, and other outputs are held. If similarly a high-level signal is added to the terminal 981, making the terminal 971 into a low level, whenever a clock signal will be added to the input terminal 991, only the high-level terminal which is most in left-hand side in the output terminals 961–966 changes to a low level, and other outputs are held. Therefore, when the signal which appears in the output terminals 961–966 was given as a control signal of the variable delay circuit shown in drawing 1 – drawing 5 and a high-level signal is added to the terminal 971. Whenever a clock signal is added to the terminal 991, when a time delay becomes long and a high-level signal is added to the terminal 981, whenever a clock signal is added to the terminal 991, it is controlled so that a time delay becomes short. Since 1 bit of output signals change the circuit of drawing 9

at a time, if it is used for control of the variable delay circuit of drawing 1 – drawing 4, a fear of occurring at once will not have the time delay change more than the minimum resolution. Although drawing 9 showed the case where a control signal was 6 bits, it can fluctuate the number of bits of a control signal arbitrarily by fluctuating the number of the portions enclosed with the dashed line of the figure.

[0021]The 7th example of the variable delay circuit by this invention is shown in drawing 8. The circuit of drawing 5 has the fault that the number of the elements which constitute a control circuit in proportion to the number of the preset value of a time delay increases so that it may mention later. It is that with which this fault was compensated, when the desired time delay of this example is close to minimum delay time, it is operated like the circuit of drawing 5, and it uses together the conventional variable delay circuit where a control circuit is simple to enlarge a time delay. An inverter circuit for 501–506, and 701 to double a selector circuit, and for 522–527 double the polarity of a clock signal in drawing 8. It is a control terminal into which 551 inputs the input terminal of a clock signal into, and, as for the output terminal of a clock signal, 561–566, and 761–765, 552 inputs a control signal. 710 is a simple variable delay circuit of control, for example, can use a variable delay circuit as shown in drawing 9. In this example, the number of stages of the selector circuits 501–506, It sets up so that total of the time delay of the portion which consists of the selector circuits 503–506 and the inverter circuits 522–527 may be comparable as the minimum delay time of the variable delay circuit 710, and the resolution of time delay control or may become more than it. The circuit of this example carries out the same operation as the circuit of drawing 5, when the control signal that the side by which direct continuation is carried out to the input terminal 551 among the inputs of the selector circuit 701 is chosen is added to the control terminal 761. On the other hand, the control signal that the selector circuit 701 chooses the output (node 751) of the variable delay circuit 710 as the control terminal 761 is added, And when the control signal that the selector circuit 501 chooses the output (node 511) of the selector circuit 502 as the control terminal 161 is added, the time delay of the variable delay circuit 710 will be added. That is, in this example, when the selector circuit 501 chooses the signal from the input terminal 551, it becomes minimum delay time, and it becomes only a time delay for one step of the selector circuit 501. This is the same as the minimum delay time of the circuit of drawing 5. Maximum delay time serves as total of the time delay (the variable delay circuit 710 is maximum delay time) of all the circuits which constitute a delay circuit, and there is no useless portion which does not contribute to maximum delay time. The resolution of time delay control And the sum of the time delay for two steps of selector circuits (701 and 502), Or it becomes either the sum of the time delay per a selector circuit and inverter circuit (503 and 522 grades) or the sums of the time delay for two steps of inverter circuits (526 and 527), and is almost the same as the resolution of the circuit of drawing 5. The maximum delay time of the portion which consists of the selector circuits 503–506 and the inverter circuits 522–527 as stated previously, Since it has set up become the minimum delay time of the variable delay circuit 710 more than comparable, the variable range of a time delay before and after changing the selector circuit 701 is overlapped. The same may be said of the case where you make it increase the time delay of the variable delay circuit 710 at a time by one step. Therefore, it does not become larger than any whose resolution of time delay control is the above-mentioned three.

[0022]Drawing 9 shows an example of the composition of the variable delay circuit 710. In drawing 9, it is an inverter circuit group for 801–804 to make a selector circuit and for 821–824 make delay time difference. The same number as drawing 5 is given to the portion which is common in drawing 5. The circuit of drawing 9 with the control signal given to the control terminals 762–765 of each selector circuits 801–804. The course (course of only the time delay of a selector circuit) in which a time delay is short, and a long course (course used as a selector circuit and the sum of the time delay of an inverter circuit group) can be chosen now, respectively. The time delay of the inverter circuit group 822 so that it may become a value somewhat smaller than the twice of the time delay of the inverter circuit group 821, So that the time delay of the inverter circuit group 823 may serve as a value somewhat smaller than the twice [about] of the time delay of the inverter circuit group 822, And if it sets up, respectively so that the time delay of the inverter circuit group 824 may serve as a value somewhat smaller than the twice [about] of the time delay of the inverter circuit group 823, By setting up the control signals 762–765 suitably, it is possible to control the time delay of the inverter circuit group 821 freely as the minimum resolution. The minimum delay time of this circuit serves as the sum of the time delay of the selector circuits 801–804, and maximum delay time becomes what added the time delay of the inverter circuit groups 821–824 to this.

[0023]Drawing 10 shows one example of the control circuit which generates the control signal to the variable delay circuit of the 7th example mentioned above. In drawing 10, the circuit of the composition as drawing 9 in which a flip-flop circuit and 1002 are almost the same as for 1001, and 1003 are UP/DOWN counters. 961–966, and 1061–1065 are the output terminals of the control signal given to the variable delay

circuit of drawing 7, and they are connected to the control terminals 561–566 of the circuit of drawing 8, and 761–765, respectively. The terminal which inputs a signal for 971,981 to fluctuate a time delay, and 991 are terminals which input the clock signal of a low frequency wave in order to operate this circuit.

[0024]Drawing 11 (a) shows an example of the UP/DOWN counter 1003. The same number as drawing 10 is given to the portion which is common in drawing 10 in drawing 11 (a). Although the signal with which this circuit is outputted [both] to the output terminals 1062–1065 when the nodes 1072 and 1081 are set to a low level does not change, When the node 1072 is high level and the node 1081 is a low level, whenever a clock signal is added to the terminal 991, the signal of the binary number outputted to the output terminals 1062–1065 counts up one every count. On the contrary, when a low level and the node 1081 have the high-level node 1072, whenever a clock signal is added, one every count is counted down. This counter is constituted so that the signal with which all the signals outputted to the output terminals 1062–1065 were added to the node 1072 when high-level may be controlled. It is constituted so that the signal added to the node 1081 may be controlled, when similarly all outputs are low level. This has become as [produce / the malfunction accompanying overflow or underflow].

[0025]Drawing 11 (b) shows the composition of the circuit 1002, and has the almost same composition as the circuit of drawing 7. In drawing 11 (b), the same number as drawing 7 and drawing 10 is given to the portion which is common in drawing 7 and drawing 10. In the circuit 1002, only conditions for the signal outputted to the output terminal 961 to change from high level to a low level differ from the circuit of drawing 7. In the circuit 1002, only when the node 1073 is high level (therefore, the output signal of the output terminal 1061 of drawing 10, low level), the signal outputted to the output terminal 961 may change from high level to a low level.

[0026]In drawing 10, while adding the signal of a low level to the terminals 971 and 981, the control signal outputted to the output terminals 961–966 like the case of drawing 7 does not change. The internal nodes 1071–1072 and 1081 also serve as a low level altogether in this case, and the control signal outputted to the output terminals 1061–1065 does not change, either. Here, the case where the signal added to the terminal 971 making the terminal 981 into a low level is made high-level is considered. If there is at least one thing of a low level in the terminal of the output terminals 961–966 at this time, The signal altogether outputted to the output terminals 1061–1065 with a low level does not change, but the internal nodes 1071–1072 and 1081 change like the case where only the signal outputted to the output terminals 961–966 is drawing 9. When the output of the output terminal 1061 was a low level, the output terminals 961–966 were altogether set to high level and a clock signal is added to the terminal 991 next, the output terminal 1061 changes high-level. The signal outputted to the terminals 1062–1065 at this time does not change. If all the signals outputted to the output terminals 961–966, and 1061 are set to high level, whenever a clock signal is added to the terminal 991 from the next, the signal of the binary number outputted to the output terminals 1062–1065 will count up one every count. And if all the signals outputted to the output terminals 961–966, and 1061–1065 are set to high level, it will not change any more.

[0027]Next, the case where the signal added to the terminal 981 making the terminal 971 into a low level is made high-level is considered. If there is at least one high-level thing in the signal outputted to the output terminals 962–966 at this time, the signal with which the internal nodes 1071–1072 and 1081 are altogether outputted to the output terminals 1061–1065 with a low level will not change. At this time, it changes like [the signal outputted to the output terminals 962–966] the case of drawing 9. If all the signals outputted to the output terminals 962–966 are set to a low level, it will not be concerned with the state of the terminal of the output terminal 961–1061, but the internal node 1081 will become high-level. Therefore, whenever a clock signal is added to the terminal 991 from the next, the signal of the binary number outputted to the terminal of the output terminals 1062–1065 counts down. While the signal outputted to the output terminal 1061 has at least one high-level signal in the output terminals 1062–1065, it does not change, but if all of the output terminals 1062–1065, and 962–966 are set to a low level, Next, when a clock signal is added, if the signal currently then outputted to the output terminal 1061 is high-level, the output terminal 1061 will change to a low level. Although the output terminal 1061 does not change between high level, the output terminal 961 will change to a low level, when a clock signal is added next, if all of the output terminal 1061, and 962–966 are set to a low level. And if all the signals outputted to the output terminals 961–966, and 1061–1065 are set to a low level, it will not change any more. Thus, a control signal is made to change until the time delay of the request with a change is suitably acquired in the signal added to the terminals 971 and 981.

[0028]If the variable delay circuit of drawing 8 is controlled using the above circuits, it will be controlled to separate, after making a time delay into the minimum previously, when making a time delay increase and separating, after connecting this variable delay circuit 710 previously, when using the portion of the variable

delay circuit 710.

[0029]When the circuit of drawing 7 is compared with the circuit of drawing 11 (a), the circuit of drawing 11 (a) can perform 16 steps (it is an n -th power stage of 2 in n bit) of control at 4 bits to the circuit of drawing 7 performing seven steps (it is $n+1$ step in n bit) of time delay control at 6 bits. Since the circuit of drawing 9 is [most circuits of drawing 11 (a)] also that it is the same (the amount of resources of a flip-flop circuit occupies most), when controlling a multi stage story, the circuit of drawing 11 (a) of the circuit structure per bit is more nearly small-scale, and it ends. However, a complicated decoder is needed when it is going to control variable delay circuits, such as drawing 5, by the circuit of drawing 11 (a). Therefore, if a variable delay circuit like drawing 8 is controlled by the control circuit which combined both circuits like drawing 10, a variable delay circuit with the advantage of the circuit of drawing 5 can be realized, without enlarging circuit structure not much.

[0030]Next, the clock phase adjusting device used for a computer system etc. is explained as an example to which the variable delay circuit described above is applied.

[0031]Drawing 12 is a lineblock diagram showing one example of a clock phase equalization circuit. In drawing 12, it is a distribution destination where 1200 receives the supply source of a clock signal and 1210 receives the clock signal. 1220 is a logic circuit group which performs information processing etc. using a clock signal, and is arranged ranging over two or more distribution destinations 1210. The high-frequency oscillator which generates the signal of high frequency with which 1201 in the clock signal supply source 1200 becomes a source of a clock signal, The clock signal generating circuit which generates a clock signal and a reference signal from the high frequency signal with which the high-frequency oscillator 1201 outputs 1202, A buffer circuit for 1203 to send a clock signal and a reference signal to each distribution destination 1210 and 1231 are wiring for sending a clock signal and a reference signal to each distribution destination 1210. 1211 in each distribution destination 1210 is a phase adjustment circuit which adjusts the phase of a clock signal using a reference signal, and the variable delay circuit mentioned above is used into this. 1212 is a buffer circuit for sending the clock signal by which phase adjustment was carried out to the logic circuit group 1220. In order to generate a reference signal in this circuit or to perform phase adjustment, the sequence signal for deciding the reference signal then sent and the variable delay circuit which should be adjusted is required. When the whole system of drawing 12 is controlled by other computers and moves, it is also possible to send a sequence signal from the computer, but. Even when the system of drawing 12 is independent, in order to make operation possible, the sequential circuit which generates a sequence signal from a reset signal etc. is required in the clock signal generating circuit 1202. A buffer circuit for the terminal into which 1251 inputs the reset signal for it, etc., and 1204 to send a sequence signal to each distribution destination 1210, and 1232 are wiring for sending a sequence signal to each distribution destination 1210. The signal (what is called a power on reset signal) which will be outputted if power supply voltage is stabilized after a power switch, the reset signal which operates a switch etc. manually and is sent when a certain abnormalities occur to a device, etc. can be used for the reset signal inputted into the terminal of 1251.

[0032]Although it changes with the accuracy and the ranges of phase adjustment, since the scales of the phase adjustment circuit 1211 are about 1000 – thousands gates, when the scale of one logic LSI is thousands of or less gates, the wiring board etc. in which two or more LSI was carried become the one distribution destination 1210. However, one LSI can also be made into the one distribution destination 1210 if the scale of one logic LSI will be 10,000 or more gates. In big LSI of a scale, it can also have two or more distribution destinations 1210 in one LSI. The wiring 1231 is possible also when it is wiring of the metal membrane constructed on the wiring board, also when it is wiring by a cable etc., it is possible, but. the wiring 1231 of the side (also side which will send a clock signal if it can do) which sends a reference signal at least has the if possible equal propagation time of a signal (to isometry [Electrically]) — it designs like. Since a clock signal and a reference signal are high-speed signals and are a signal with which phase precision is also demanded, it is desirable to use the high circuit of driving ability for the buffer circuit 1203. On the other hand, since a sequence signal is a far late signal, a not much high thing has necessity in neither the driving ability of the buffer circuit 1204, nor the isometry nature of the wiring 1232.

[0033]Two or more flip-flop circuits 1221 are in the logic circuit group 1220, and synchronizing with a clock signal, when a signal transmits between flip-flop circuits, information processing etc. are performed. Therefore, if the phase of the clock signal supplied to each flip-flop circuit shifts from a predetermined phase above to some extent, a possibility of causing malfunction to information processing will arise. The limit of phase difference where the flip-flop circuit of which high-speed operation is required especially is permitted becomes small. In this example, in order to prevent this phase difference, all the phases of the clock signal supplied to two or more flip-flop circuits 1221 which establish the phase adjustment circuit

1211 in each distribution destination 1210, and are in two or more distribution destinations 1210 are doubled with a predetermined phase. Below, the phase adjustment circuit 1211 and clock signal generating circuit 1202 grade are explained.

[0034] Drawing 13 shows one example of the phase adjustment circuit 1211. The input buffer circuit of LSI in which 1301 carries this circuit in drawing 13, A control circuit for 1302 and 1303 to control a variable delay circuit, and for 1312 and 1313 control the variable delay circuits 1302 and 1303, It is a decoder circuit for 1305 to supply a selector circuit and for 1306 supply a frequency divider and a signal [need / a phase comparison circuit and 1308 / for the control circuit 1304 or selector circuit 1305 grade / 1307]. Wiring for 1321 to transmit the clock signal of the 1st phase used by the logic circuit group 1220, Wiring for 1322 to transmit the clock signal of the 2nd phase used by the logic circuit group 1220, the terminal into which 1350 inputs a clock signal, the terminal into which 1351 inputs a reference signal, and 1352 are terminals which input a sequence signal.

[0035] Here, it is for the variable delay circuit 1302 amending the phase difference of the clock signal resulting from the temperature change etc. which were produced during operation of the logic circuit group 1220, for example, the variable delay circuit which a spike shape noise as shown in drawing 1 – drawing 4 does not generate is used. It is for the variable delay circuit 1303 amending the fixed phase difference resulting from the manufacturing variation of a semiconductor device, etc., and the big variable delay circuit of a variable range as shown in drawing 5 or drawing 7 is used. The change of the time delay of the variable delay circuit 1303 is performed after receiving a reset signal etc. before the logic circuit group 1220 begins to work. The circuit etc. which were shown in drawing 7 or drawing 10 as the control circuit 1312–1313 according to the variable delay circuit 1302 or the kind of 1303 are used. The selector circuit 1305 is a circuit for choosing the clock signal of the phase which is the target of a phase comparison out of the clock signal sent to the logic circuit group 1220, for example, a circuit as shown in drawing 6 is used. The frequency divider 1306 carries out dividing of the clock signal added to the clock signal input terminal 1350, and generates the clock signal of a low frequency wave required for the control circuit 1312–1313 or phase comparison circuit 1307 grade. About 8 dividing may be sufficient as the division ratio of the frequency divider 1306, for example. The phase comparison circuit 1307 is a circuit which compares the phase of the clock signal sent to the logic circuit group 1220 with the phase of the reference signal added to the reference signal input terminal 1351. According to sequence signals (information etc. which shows whether it is the stage to work the kind and the logic circuit group 1220 of a reference signal which have been then sent), the decoder circuit 1308, Decide whether decide whether to transmit the clock signal of which phase to the phase comparison circuit 1307 from the selector circuit 1305, and to transmit the output of the phase comparison circuit 1307 to which control circuit 1312–1313, and. It is a circuit for supplying the signal 1320 which determines whether the logic circuit group 1220 is worked. The details of the phase comparison circuit 1307 and the decoder circuit 1308 are later mentioned to drawing 14 and drawing 15.

[0036] An example of the phase comparison circuit 1307 is shown in drawing 14. In drawing 14, the terminal into which 1541 inputs a reference signal, the terminal which inputs the clock signal with which 1452 was chosen in the selector circuit 1305, and 991 are terminals which input the clock signal of the low frequency wave generated by the frequency divider 1306. When 1471 and 1481 are terminals which output a decision result and the clock signal inputted into the terminal 1452 is earlier than the reference signal inputted into the terminal of 1451 (the time delay of a variable delay circuit is made to increase), When the clock signal inputted into the terminal 1452 is later than the reference signal inputted into the terminal 1451 for the terminal 1471 again (the time delay of a variable delay circuit is decreased), a signal is outputted to it at the terminal 1481. 1401 is two 2 input NAND circuits by which cross connection was mutually carried out in input and output, and judges the forward delay relation of the phase of a reference signal and a clock signal for every cycle. A flip-flop circuit for 1402 to hold the decision result of 2 input NAND circuit 1401 between one cycle, A flip-flop circuit for 1403 to equalize load added to 2 input NAND circuit 1401, 1404 delays the output of 2 input NAND circuit 1401 for a while by gate delay, The circuit for creating the timing signal which operates the flip-flop circuit 1402 certainly, 1405 incorporates the output of the flip-flop circuit 1402 with the cycle of the clock signal of a low frequency wave into which it was inputted from the terminal 991, and it is a flip-flop circuit group for preventing malfunction by the output of the flip-flop circuit of the preceding paragraph being held with a mean value. 1406 is 4 bit counter circuits which a count follows with the cycle of the low frequency clock signal inputted from the terminal 991, it follows the output of the flip-flop circuit group 1405, and a count follows it only the counter 1406 of a gap or one of the two. This circuit is provided in order to keep that signal from getting across to a latter circuit, even if 2 input NAND circuit 1401 performs an erroneous decision suddenly under the influence of a noise etc. 1407 is a flip-flop circuit which holds the decision result after passing along the counter circuit 1406 between

one cycle of a low frequency clock signal. The counter circuit 1406 is realizable also in a circuit as shown, for example in drawing 11 (a). However, if the node 1464 becomes high-level, it shall constitute so that all the flip-flop circuits in the counter circuit 1406 may be reset and it may become the oar 0. Here, one count number of the counter circuit 1406 amounts to 15, and an output presupposes that it became all ones and either of the internal node 1462 or 1463 was set to a low level. Although the signal which makes the output terminal 1471 or 1481 fluctuate the time delay of a variable delay circuit at this time as the count number of the counter circuit 1406 of another side is 11 or less is outputted, When the count number of the counter circuit 1406 of another side also amounts to 12 or more, the output terminals 1471 and 1481 are still low level. If one count number amounts to 15, the node 1464 becomes high-level, and both counter circuits 1406 will be reset and, in any case, it will be recounting from 0. That is, if the incidence of the decision result of 2 input NAND circuit 1401 inclines toward either by the 15:11 or more ratio, the signal which makes the time delay of a variable delay circuit fluctuate will be outputted, but if it is a 15:12 [less than] ratio, the signal which it is considered mostly that is the same number and changes a time delay will not be outputted. About the detailed principle of the phase comparison circuit of drawing 14, it is indicated by JP,2-168308,A, for example.

[0037]One example of the decoder circuit 1308 in drawing 13 is shown in drawing 15. In drawing 15, 1301 is the input buffer circuit connected to the sequence signal input terminal 1352. It is a flip-flop circuit for 1501 synchronizing with 3 input NAND circuit, 1502 synchronizing with 4 input NAND circuit, and 1503 synchronizing a sequence signal with a low frequency clock signal, and incorporating. The terminal into which the sequence signal which the reference signal with which 1551 is then sent tells the thing showing the phase of the clock signal of the 1st phase or the thing showing the phase of the clock signal of the 2nd phase is inputted, The terminal into which the sequence signal which 1552 tells the stage of initial adjustment or the stage of operating status is inputted, and 1553 are terminals into which the sequence signal which tells whether it is a stage from which it is moving to other states is inputted from the state where there are other sequence signals and reference signals. The selector circuit 1305 is controlled based on the sequence signal inputted into the terminal 1551 to be shown in a figure, and it is controlled whether the signal from a phase comparison circuit is told to the control circuit 1312-1313 of which phase. The signal which shows whether it is at the initial adjustment time is told with the logic circuit group 1220 based on the sequence signal inputted into the terminal 1552 in the control circuit 1312-1313. In each control circuit 1312, "0" is reset for the flip-flop circuit of shoes to set that this signal becomes high-level beforehand, and other flip-flop circuits are set to "1." The delaying amount of the variable delay circuit 1302 is set as the center (or suitable value defined beforehand) of a variable range by this, and is fully secured in the adjustable range at the time of operation. This state continues until initial adjustment finishes. If initial adjustment finishes, the control circuit 1312 will start the usual control action, and the signal to which a time delay is changed stops going to the control circuit 1313, and the control signal at the time of the end of initial adjustment is held. The signal which shows that it was in operating status is told to the logic circuit group 1220. When the state of these sequence signals and reference signals changes, the sequence signal added to the terminal 1553 is set to a low level, is kept from going the signal which fluctuates a time delay to every control circuit 1312-1313, and prevents malfunction.

[0038]One example of the clock signal generating circuit 1202 of drawing 12 is shown in drawing 16. The flip-flop circuit for 1601 carrying out dividing of the output of the high-frequency oscillator 1201, and making the frequency of a clock signal in drawing 16. A flip-flop circuit for 1602 to make two signals with the same phase contrast as the phase contrast of the clock signal of the 1st phase and the 2nd phase, 1603 chooses either of the outputs of the flip-flop circuit 1602 according to a sequence signal, The flip-flop circuit for doubling the SREKU circuit for generating a reference signal, and 1604 with predetermined phase relation by synchronizing a clock signal and a reference signal with the output of a high-frequency oscillator, Before 1605 sends a reference signal to each distribution destination 1210, it is delayed uniformly beforehand, The delay element for taking the time delay of a clock signal and balance by the buffer circuit 1212 in the distribution destination 1210, and the variable delay circuits 1302 and 1303 in the phase adjustment circuit 1211, The sequential circuit where 1606 generates a sequence signal, and 1607 are frequency dividers which generate the clock signal of the low frequency wave for operating a sequential circuit. The terminal in which 1651 outputs a clock signal, the terminal in which 1652 outputs a reference signal, the terminal which outputs the sequence signal which supplies 1661-1663 to the terminals 1551-1553 of drawing 15, respectively, and 1251 are terminals which input a reset signal. The division ratio of the frequency divider 1607 is larger than the frequency divider 1306 of drawing 13, for example, uses the thing before and behind 1024 dividing. If the edge one or more cycles before a clock signal is doubled with a reference signal instead of delaying a reference signal by the delay element 1605, the delay element 1605

is not necessarily required.

[0039] Drawing 17 shows one example of the sequential circuit 1606. A flip-flop circuit for 1701 to incorporate the reset signal inputted into the terminal 1251 in drawing 17 synchronizing with the clock signal of the low frequency wave supplied from the frequency divider 1607. The flip-flop circuit for resynchronizing with the clock signal again same in order that 1702 may not cause malfunction when the output of the flip-flop circuit 1701 is held with the middle value of high level and a low level (when what is called a hazard occurs). They are a frequency divider which makes the signal for 1703 carrying out dividing of the clock signal of a low frequency wave further, and changing a reference signal with a constant period, and a flip-flop circuit which makes the sequence signal which decides whether 1704 is carrying out 2 dividing of the signal, and sends the reference signal of the phase of a gap. 1705-1707 are flip-flop circuits which constitute the shift register circuit which operates synchronizing with the clock signal which is a low frequency wave which the frequency divider 1607 outputs. It is for making the signal (signal outputted to the terminal 1661) which changes a reference signal, and the signal (signal outputted to the terminal 1663) used as the index of being under the change of a reference signal. The flip-flop circuit for detecting that the signal which changes a reference signal after the reset signal inputted into the terminal of 1251 is canceled took a round of 1708, 1709 and 1710 are the flip-flop circuits for changing the signal synchronizing with the signal outputted to the terminal 1661. The high-level signal is always added to the terminal 1750 linked to the flip-flop circuit 1708. The division ratio of the frequency divider 1703 is set up become more than the time that needs the cycle of the output of this frequency divider for time delay adjustment of the variable delay circuit 1303 in drawing 13. In 1280 steps and the frequency divider 1306, the counter circuit 1406 of 8 dividing and drawing 14 For example, four bit counters (16 dividing), [the change range of the time delay of the variable delay circuit 1303] Supposing the division ratio by the flip-flop circuit 1601 of drawing 16 is 2 dividing and the frequency divider 1607 is 1024 dividing, the division ratio of the frequency divider 1703 should just be more than 320 ($1280 \times 8 \times 16 \times 2 / 1024$). What is necessary is for a frequency divider to be easy to constitute if it is made for a division ratio to serve as a exponentiation of 2, and just to make it into 512 or more dividing, when it is this example. However, it is [the variable width of the variable delay circuit 1302 in drawing 13] smaller to constitute so that time may be gained, and ends until it enlarges a division ratio further practically and the temperature of the whole device is stabilized to some extent.

[0040] In drawing 17, the output of the flip-flop circuit 1702 is high-level between high level, and, as for the frequency divider 1703 and the flip-flop circuit 1704-1708, all will be reset by the reset signal inputted into the terminal 1251. Here, if the reset signal inputted into the terminal 1251 is set to a low level, the output of the flip-flop circuit 1702 will serve as a low level, and reset of the frequency divider 1703 and the flip-flop circuit 1704-1708 will be canceled. Then, the frequency divider 1703 begins to move and the flip-flop circuit 1708 will be in the state of waiting for the edge of the standup of a signal to appear in the node 1751. Since the node 1751 is already high-level immediately after canceling a reset signal, that the output of the flip-flop circuit 1708 changes. Once the signal which appears in the node 1751 is set to a low level, it is a time (namely, after the signal which changes a reference signal takes a round) of becoming high-level again. As for the output of the flip-flop circuit 1708, high level is held unless the reset signal again inputted into the terminal 1251 becomes high-level after that. Since one step of signal which appeared in the node 1751 is shifted at a time by the shift register circuit which the flip-flop circuits 1705-1707 constitute, It is detectable whether the output of the flip-flop circuit 1706 which exists in the meantime changes with the exclusive OR of the output of the flip-flop circuits 1705 and 1707. The clock signal and sequence signal of a polyphase which were adjusted to the desired phase by the clock phase adjusting device 1200 of drawing 12 as mentioned above can be supplied to two or more distribution destinations 1210.

[0041] Drawing 18 shows other examples of the clock signal generating circuit 1202, and shows one example of the clock signal generating circuit 1202 used when supplying the clock signal of four phases to the logic circuit group 1220. The point that the flip-flop circuit 1601 which the circuit shown in drawing 18 carries out dividing of the output of the high-frequency oscillator 1201, and makes the frequency of a clock signal constitutes the frequency divider of 4 dividing. The point constituted so that the flip-flop circuit 1602 which makes a signal with the same phase contrast as the phase contrast of a clock signal may output the signal for four phases. It differs from the circuit shown in drawing 16 in the point that 2 bits of sequence signals (signal outputted to the terminal 1661) which choose the phase outputted as a reference signal are needed, the point made the composition as which the selector circuit 1603 which chooses the phase outputted as a reference signal chooses one from four signals, etc. In drawing 18, the same number as drawing 16 is attached about the portion which has the same function as drawing 16. The selector circuit 1603 also has composition which chooses one at a stretch from four signals in the selector circuit

of 4 to 1. When you need the high-speed clock signal that a signal does not arrive to the flip-flop circuits 1602-1604 in the time delay of the selector circuit of 4 to 1, It can be shortened even to the time delay of the selector circuit of 2 to 1 by having composition which passes along two steps of selector circuits of 2 to 1, as shown in drawing 18, and inserting the flip-flop circuit 1801 in between.

[0042]Drawing 19 shows the example of further others of the clock signal generating circuit 1202, The clock signal generating circuit used when tuning finely on the actually used frequency, after a clock signal with low frequency performs the coarse control of the time delay of the variable delay circuit 1303 of drawing 13 first is shown. The flip-flop circuit which constitutes a frequency divider for 1901 to make the clock signal of the low frequency wave for coarse controls in drawing 19, A flip-flop circuit for 1902 to make the output of the flip-flop circuits 1901 and 1601 the signal in sync with the output of the high-frequency oscillator 1201 and 1903 are the selector circuits for changing the clock signal of the low frequency wave for coarse controls, and the clock signal of the actually used frequency. 1961 is a terminal which outputs the sequence signal which shows whether it is a period of a coarse control, or it is a period of fine adjustment. Even if there is no telling whether to be a period of a coarse control or be a period of fine adjustment, in each distribution destination 1210, phase adjustment is possible, but. If it has composition which fixes to constant value a control signal with small time delay variation width of a variable delay circuit (for example, control signal added to the terminal of 162-166 of drawing 7) at the time of a coarse control, the time concerning a coarse control can be shortened.

[0043]Drawing 20 shows one example of the sequential circuit 1606 used for the clock signal generating circuit shown in drawing 19, for example. The point constituted so that the point that the circuit of drawing 20 differs from the circuit of drawing 17 might make two pieces the flip-flop circuit 1704 which makes the sequence signal (sequence signal outputted to the terminal 1661) which determines the phase outputted as a reference signal and a 2-bit signal might be outputted, It is the point of having formed the flip-flop circuit 2001 which detects the sequence signal other than the flip-flop circuit 1709 to detect having *(ed) the sequence signal outputted to the terminal 1661 having taken a round two times. And the variable delay circuit which controls mark adjustment by the place which was finely tuned in the second *(ed) and was ended in the second *(ed) to a round eye is changed to 1302 from 1303, and the logic circuit group 1220 is made into operating status. If it enables it to detect that the sequence signal *(ed) three times similarly, only the variable delay circuit to control is changed, and after ending in the third *(ed), it can also have composition which makes the logic circuit group 1220 operating status in the place ended in the second *(ed).

[0044]Drawing 21 shows the example of further others of the clock signal generating circuit 1202, and saves the amount of resources of the wiring which multiplexes the output terminal of a clock signal, and the output terminal of a reference signal, and connects between the clock signal supply source 1200 and each distribution destination 1210, and a terminal (signal pin of LSI). In drawing 21, 2101 is a selector circuit and 2102 is a flip-flop circuit. The point that the circuit of drawing 21 differs from the circuit of drawing 19 is a point which forms the selector circuit 2101 and enabled it to output both a clock signal and a reference signal to the terminal of 1651. And when, sending the signal which is equivalent to the phase of the clock signal of the 1st phase or the 3rd phase as a reference signal for example, a clock signal is sent from upper terminal 1,651' by drawing 21, and a reference signal is sent from lower terminal 1,651'. *(ed) which sends a clock signal from terminal 1651' of the drawing 21 bottom conversely, and sends a reference signal from upper terminal 1651' when sending the signal which is equivalent to the phase of the clock signal of the 2nd phase or the 4th phase as a reference signal. If it does in this way, the wiring for sending a reference signal, etc. can save 1 set. The flip-flop circuit 2102 is needed when a signal does not arrive from the flip-flop circuit 1801 to the flip-flop circuit 1604 via the selector circuits 1603 and 2101 among one cycle of the output of the high-frequency oscillator 1201. The method of generating the clock signal for supplying the logic circuit group 1220 from the clock signal and reference signal which were carried out in this way and sent is later mentioned to drawing 26.

[0045]Drawing 22 shows the example of further others of the clock signal generating circuit 1202, and after the phase adjustment of a clock signal is completed before working the logic circuit group 1220, it is made to stop a clock signal once. If this circuit is used, even if the course which transmits a sequence signal has a skew, it will become possible to start the flip-flops in the logic circuit group 1220 all at once. In drawing 22, the sequence signal which accepts it after phase adjustment ends 2251 until it goes into operating status, and becomes high-level, and 2200 are clean start circuits. Although the signal which carried out dividing of the output of the high-frequency oscillator 1201 like the flip-flop circuits 1601-1901 and 1902 of drawing 19 or drawing 21 is outputted between low level, the sequence signal 2251 the clean start circuit 2200, When the sequence signal 2251 becomes high-level, it is constituted so that an output may be

set to a low level. The sequence signal 2251 provides one more step of flip-flop circuit behind the flip-flop circuit 1710–1711 connected from the flip-flop circuit 2001 of drawing 20, for example, Only when the output of the 1st step of flip-flop circuit 1710 and the 3rd step of added flip-flop circuit is not in agreement, it can create, as the sequence signal 2251 becomes high-level.

[0046]Drawing 23 is a lineblock diagram showing an example of the clean start circuit 2200. In drawing 23, 2201 incorporates the sequence signal inputted from the terminal 2251 synchronizing with the output of the high-frequency oscillator 1201, and. The flip-flop circuit for preventing generating of a hazard and 2202 are NOR circuits for the output of the flip-flop circuit 2201 to make the clock signal which stops between high level. This circuit carries out dividing of the clock signal with which the output of the flip-flop circuit 2201 is outputted via NOR circuit 2202 between low level in the flip-flop circuit 1601–1901 one by one, The output which synchronized with the output of the high-frequency oscillator 1201 in the flip-flop circuit 1902 is sent to the selector circuit 1903. However, when the output of the flip-flop circuit 2201 becomes high-level, the output of NOR circuit 2202 is fixed to a low level, and the flip-flop circuit 1601 is reset and an output is fixed to a low level. If the output of the flip-flop circuit 2201 is again set to a low level here, the flip-flop circuit 1601 will start operation of dividing again. In these operations, the moment the output of the flip-flop circuit 2201 changes, another input of NOR circuit 2202 is, immediately after becoming high-level, and when the sequence signal 2251 changes, a spike shape noise is not outputted from NOR circuit 2202.

[0047]Drawing 24 shows the example of further others of the clock signal generating circuit 1202, and changes and sends frequency in the time of the time of a coarse control and fine adjustment of a clock signal, and a reference signal is constituted so that a signal with always low frequency may be sent. As opposed to using the output of the selector circuit 1903 for both a clock signal (signal outputted from the terminal 1651), and a reference signal (signal outputted from the terminal 1652) in the circuit of drawing 19, In the circuit of drawing 24, the output of the selector circuit 1903 was used only for the clock signal, and the output of the flip-flop circuit 1902 which always outputs the low signal of a cycle to a reference signal is directly connected with the flip-flop circuit 1602. The flip-flop circuit 2301 is for doubling the phase relation of the signal outputted as the signal and reference signal which are outputted as a clock signal. If frequency is set to not less than 200–300 MHz especially to a clock signal, it will become difficult to transmit a reference signal with the exact phase which is the same frequency. In such a case, if a circuit like drawing 23 is used, the reference signal at the time of fine adjustment can be sent on the same frequency as the time of a coarse control. The method of generating the clock signal for supplying the logic circuit group 1220 from the clock signal and reference signal which were carried out in this way and sent is later mentioned to drawing 27.

[0048]Drawing 25 shows the example of further others of the clock signal generating circuit 1202, and enables it to transmit the clock signal of frequency different every distribution destination 1210. In the circuit shown in drawing 24, this circuit forms the selector circuit 1903 and 1 more set of flip-flop circuit 2301, and can also supply now the clock signal of the frequency for 2 more minutes which carried out 1 dividing. In order that the speed of a circuit may link with performance directly, there is a portion (for example, central processing unit) which needs as high-speed a circuit as possible, and even if speed is as slow as a few, a portion (for example, input/output device) to constitute from a cheap element is in the logic circuit group 1220. In this case, at the former, although a high-speed clock signal is needed, by the latter, it may also happen not to operate, if it is not a low-speed clock signal. In such a case, the circuit of drawing 25 is effective, a high-speed clock signal can be supplied to some distribution destinations 1210, and the clock signal of the frequency of 1/the 2 can be supplied to other distribution destinations 1210. The reference signal should just supply a signal common to any distribution destination.

[0049]Drawing 26 shows the example of further others of the clock signal generating circuit 1202, and it uses it to supply the clock signal (for example, 800 MHz and 600 MHz) of two kinds of frequency which is not in the relation between a multiple and a divisor mutually. or [in this case, / that it is realizable even if the oscillator of the frequency of the least common multiple (this example 2400 MHz) of two kinds of this frequency is provided and it carries out dividing of that output, but the circuit which operates on that frequency is unrealizable] — or when becoming very expensive, the circuit of drawing 26 can realize. In drawing 26, it is a delay circuit where 2501 transmits a multiplying circuit and 2502 transmits a signal by the phase adjustment circuit and the time delay in which a frequency divider and 2504 are in general equal to the frequency divider 2503 as for 2503. 2505 is the same circuit as the portion which comprises the flip-flop circuits 1602–1801 and 1604 and selector circuit 1603 grade in the circuit shown in drawing 19 etc. In the circuit of drawing 26, oscillating frequency of the high-frequency oscillator 1201 is made into the greatest common denominator (the above-mentioned example 200 MHz) of the frequency of two kinds of

clock signals, and is multiplied even in required frequency by the multiplying circuit 2501. In the case of this example, it is 3 multiplying and 4 multiplying, but it is clear that four multiplying circuits' it can constitute from two steps of two multiplying circuits. Thus, by the phase adjustment circuit 2502, the created signal (600 MHz and 800 MHz) is doubled with the phase of a 200-MHz signal, and is outputted as a clock signal. The frequency divider 2503 and the selector circuit 1903 are circuits which generate and choose a signal required like the circuit which the frequency divider and selector circuit 1903 grade which the flip-flop circuit 1901 constitutes in drawing 19 etc. constitutes in order to perform a coarse control or fine adjustment, and supply it. The equivalent delay circuit 2504 is formed in order to double the time delay of the signal path at the time of a coarse control, and the signal path at the time of fine adjustment in general. There is no course which is inputted into the selector same after the signal of maximum frequency separates into two in the circuit shown in drawing 19 etc., By the time the signal of other frequency is outputted after it is extracted to one by a selector, in order to redouble a phase with the flip-flop 1604, such an equivalent delay circuit is unnecessary, but. The signal (800 MHz and 600 MHz) itself is selected, and since it has composition outputted as it is, the equivalent delay circuit 2504 is needed in the circuit of drawing 26. Since the reference signal of the circuit of drawing 26 is shifted with an 800-MHz clock signal and is creating a 200-MHz signal, Although the reference signal equivalent to the phase of the clock signal of the 1st phase and the clock signal of the 2nd phase that reversed it can be supplied to a 600-MHz clock signal, To an 800-MHz clock signal, only the reference signal equivalent to the phase of the clock signal of the 1st phase will be supplied.

[0050]One example of the phase adjustment circuit 2502 is shown in drawing 27. In drawing 27, 2507 is a variable delay circuit and a delay circuit where delay control circuits and 2509 are delayed in a flip-flop circuit, 2510 and 2513 are delayed in a selector circuit, and, as for 2511 and 2514, 2508 delays a signal by several steps of gate circuits, and 2512 is a phase comparison circuit. In the circuit of drawing 27, after phase adjustment of the clock signal inputted into the terminal 2551 is carried out by the variable delay circuit 2507, it is outputted to the terminal 2553. Here, the phase of the signal outputted to the terminal 2553 is adjusted so that it may become early from the phase of the signal outputted to the terminal 2554 by the time delay by the flip-flop circuit 2509 and the selector circuit 2510. Therefore, if it designs so that these time delays may coincide with that by the selector circuit 1903, the frequency divider 2503, or the equivalent delay circuit 2504 of drawing 26 in general, the phase of the signal inputted into the shift circuit 2505 can be coincided in general. If either is enlarged, it is also possible to use a desired forward delay relation. The delay circuit 2511 is a circuit for shifting timing relationship so that the flip-flop circuit 2509 can incorporate certainly the signal which appears in the internal node 2555, when the signal outputted to the terminal 2553 and the signal outputted to the terminal 2554 are in the above phase relation. The selector circuit 2513 and the delay circuit 2514 are circuits for making a little phase of the signal outputted to the terminal 2554 shift and readjust, once phase adjustment is completed. When the phase of the signal inputted into the phase comparison circuit 2512 is shifted 180 degrees exactly, this circuit is needed in order to prevent also already outputting the signal of a late gap no longer, and phase adjustment not progressing. If time required for adjustment passes after starting phase adjustment, a phase will be in either the state exactly shifted 180 degrees or the state where the phase suited, and the intermediate state will be lost. If it can shift as the gap whose phase comparison circuit 2512 is 180 degrees about the signal outputted to the terminal 2554 can be distinguished here, when shifted 180 degrees, phase adjustment is started, and when correct, a part to have been shifted a little will be readjusted. Therefore, after making it readjust, it falls and wears in the state where the phase always suited, and becomes Lycium chinense. The sequence signal inputted into the terminal 2562 is a signal for performing this readjustment. The sequence signal inputted into the terminal 2563 is for resetting or setting suitably the flip-flop circuit in the control circuit 2508, and making it the time delay of the variable delay circuit 2507 become at least the middle of variable width, and before it starts the first adjustment, it performs this setting out. The sequence signal inputted into the terminal 2561 is for adjusting 1 set of two the variable delay circuits 2507 and the delay control circuits 2508 at a time, and can use the one phase comparison circuit 2512 also [phase adjustment / of both signals] with this signal. An order of changing a sequence signal performs center value setting out of the variable delay circuit 2507 with the signal first inputted from the terminal 2563, Next, the signal inputted from the terminal 2561 is changed with sufficient time interval to perform phase adjustment in the state of both high level and a low level, The signal furthermore inputted from the terminal 2562 is changed, the signal finally again inputted from the terminal 2561 is changed with sufficient time interval to perform phase adjustment in the state of both high level and a low level, and the phase adjustment of this circuit is ended. And after the phase adjustment of this circuit is completed, the sequence signal outputted to the terminals 1661-1663, and 1961 is usually changed to a passage, and the

phase adjustment circuit 1211 in each distribution destination 1210 is adjusted. The sequence signal which fixes the output of the control circuit of the portion which is not made to follow a temperature change is established separately, and after phase adjustment is completed in above order, it fixes with this signal to have composition which is made to always follow a temperature change also about the circuit of drawing 27. After that, the signal (the same signal as the signal outputted to the terminal 1661 may be used) inputted from the terminal 2561 is changed periodically, and the adjustment in each distribution destination 1210 is started.

[0051]Drawing 28 shows the circuit used when making the course which transmits a clock signal, and the course which transmits a reference signal make it serve a double purpose as other examples of the phase adjustment circuit 1211 used into each distribution destination 1210 are shown and it was shown in drawing 21. In drawing 28, 2601 is a selector circuit and the delay circuit constituted so that, as for 2602, a time delay might become equal to the selector circuit 1305. The object for 2 phases of other portions is the same as that of the circuit of drawing 13 except for the point which has become 4 phases. When performing phase adjustment using the circuit of drawing 28 and doubling the clock signal of the 1st phase and the 3rd phase, among a figure, the signal inputted from the lower input terminal 1350 is chosen by the selector circuit 2601, and is inputted into the phase comparison circuit 1307. When performing phase adjustment of the clock signal of the 2nd phase and the 4th phase, the reference signal supplied via the course of the clock signal of the 1st phase is chosen by the selector 2601, and is inputted into the phase comparison circuit 1307. Therefore, it is adjusted about the clock signal of the 1st phase and the 3rd phase, comparing the reference signal inputted into the chip like the circuit of drawing 13, and directly. About the clock signal of the 2nd phase and the 4th phase, in order to compare with the reference signal sent via the course of the clock signal of the 1st already adjusted phase, it will compare with the reference signal indirectly inputted from the input terminal 1350 of the figure bottom. Therefore, it will double with the reference signal inputted from the input terminal 1350 of the figure bottom about all the phases. Although the direction in which the course of a reference signal is provided independently cannot be overemphasized [that the accuracy of phase adjustment goes up], when you want to create the whole system cheaply, this example which can save the course of a high speed signal is effective. When control which is made to follow a temperature change in the circuit of drawing 28 at the time of operation of the logic circuit group 1220 is performed, Only as for the phase, by making it in agreement with the signal which the reference signal suitable for the clock signal of any one phase inputs from the terminal 1350 which inputs the clock signal of the figure bottom, it is possible to make it follow. What is necessary is just to add the same control signal as other phases by making the phase into a representation phase so that two or more phases may be later mentioned using drawing 30 to follow a temperature change.

[0052]Drawing 29 is a circuit used when a reference signal is transmitted on frequency lower than a clock signal, as the example of further others of the phase adjustment circuit 1211 used in each distribution destination 1210 is shown and it was shown in drawing 24. This circuit is provided with the system which performs a phase comparison when the clock signal and the reference signal have been sent on the same frequency at the time of a coarse control, and the system which performs a phase comparison when only the clock signal has been sent on high frequency at the time of fine adjustment and operation. In the circuit of drawing 29, when a clock signal and a reference signal are the same frequency, the lower phase comparison circuit 1307 is used among a figure. When the frequency of a clock signal is higher, the phase of the signal which synchronized the reference signal with the clock signal by the flip-flop circuit 2701, and the original reference signal is compared. In the circuit of drawing 29, one circuit can also be shared for the portion (flip-flop circuit 1405 of drawing 14) or subsequent ones into which 2 circuit ***** synchronizes a comparison result with the clock signal of a low frequency wave in a phase comparison circuit in the phase comparison circuit 1307. The circuit which replaces with the circuit shown in drawing 29, for example, is indicated by drawing 12 of JP,63-231516,A, drawing 15 - drawing 18, etc. can also be used.

[0053]Drawing 30 shows the example of further others of the phase adjustment circuit 1211 used in each distribution destination 1210, and saves the amount of resources of the control circuit 1312 for making a temperature change etc. follow at the time of operation. Namely, although the coarse control before making the logic circuit group 1220 into operating status, and fine adjustment are performed by adjusting the control circuit 1313 which controls the variable delay circuit 1303 as well as former one by one, When making a temperature change etc. follow at the time of operation, something doubles only the phase by making the clock signal of one phase into a representation phase. And the same control signal also as the variable delay circuit 1302 of other phases is added. If the phase adjustment circuit 1211 and the buffer circuit 1212 are in one LSI, it can be presumed that the circuit element which constitutes these circuits is

in an always in general equal temperature. Therefore, if the control signal which follows one in this is acquired, it will be thought that it can follow in general with a control signal with the same said of the others. Since the variable delay circuit of drawing 5 which changes a time delay with a gate number of stages, or drawing 7 has coarse resolution of time delay change compared with the variable delay circuit of drawing 1 which changes a time delay with the weight of load – drawing 4, as for phases other than a representation phase, phase precision will become coarse if only this finishes initial adjustment. In the circuit of drawing 30, in order to avoid this, the variable delay circuit 2801 which changes a time delay under the weight of load is added, and the resolution of the variable delay circuit 1303 is compensated. The variable width of this variable delay circuit 2801 is enough if it sets up become larger than the minimum resolution of the variable delay circuit 1303. In performing such control, after the signal (signal outputted to the terminal 1662 from the sequential circuit 1606) which decides whether to use operating status, for example becomes high-level, Only the phase can be adjusted by fixing the sequence signal (signal outputted to the terminal 1661) which decides of which phase to transmit a reference signal, transmitting the reference signal which is always equivalent to the clock signal of a representation phase. 2802 is a circuit which transmits a signal by a time delay in general equal to the input buffer circuit 1301. By this circuit, the variation for every LSI of the time delay of the input circuit 1301 can be offset, and it can hold down to the relative variation part grade of the time delay of two circuits (the input buffer 1301 and the delay circuit 2802) in LSI. If there is a portion which serves as a mutual in general equal time delay among the delay circuits 2802 and 2602, it is also possible to omit the both.

[0054]Drawing 31 shows one example of the circuit which generates the clock signal of duty 25% phase from the clock signal of the duty 50% phase obtained by examples, such as drawing 28 – drawing 30. Since the clock signal of four phases which phase adjustment was improved by accuracy can be acquired according to this invention, such a circuit is utilizable. This circuit inserts NAND circuits 2901 and 2902 between the variable delay circuit 1303 and the terminals 2651–2654 which output a clock signal, Duty 25% of the clock signal is generated by controlling the clock signal of duty 50% of each phase outputted to the internal node of 2951–2954 from the variable delay circuit 1303 with the clock signal of the following phase. By carrying out only about the edge (for example, edge of a standup) of one side of the clock signal of each phase, phase adjustment will be automatically adjusted also about another edge. Since there is a possibility that a predetermined pulse may not come out when not less than 25% of phase difference of the cycle of a clock signal is before a coarse control, The internal node 2955 is made into a low level at the time of a coarse control, it adjusts with duty 50%, the node 2955 is made high-level at the time of fine adjustment and operation, and duty 25% of the clock signal is outputted. It becomes high-level [the waveform which drawing 32 shows the signal wave form which appears in each node at this time, for example, appears in the node 2651 has the high-level node 2951, and] at the time of a low level and others, only when the node 2953 is a low level. These clock signals can be supplied also as which polar clock signal of positive/negative with the number of stages of the buffer circuit 1212. And a phase comparison is made in the same waveform as the flip-flop circuit 1221 being supplied by supplying the same signal as this also to the phase comparison circuit 1307.

[0055]Even if the selector circuit used in the circuit shown after drawing 13 inputs a signal from which an up-and-down input terminal, being outputted by the same time delay is desirable, but to the PMOS side, it is unsymmetrical and is not satisfied with the selector circuit shown in drawing 6 of this specification. Then, an example of the selector circuit which solved this problem is shown in drawing 33. In the circuit of drawing 33, put two selector circuits of drawing 6 in order and the output terminal 152 is connected in common, and it has connected so that the up-and-down input terminals 151 and 551 may cross mutually. The signal inputted from the control terminal 161 is mutually used with reverse polarity. If constituted in this way, the circuit from the input terminals 151 and 551 to the output terminal 152 becomes symmetrical mutually, and can make a time delay equal.

[0056]

[Effect of the Invention]As stated above, according to this invention, the big variable delay circuit or the variable delay circuit which a spike shape noise does not generate even if it changes a time delay working, and delay control circuits of variable width where minimum delay time is small are realizable. A clock signal can be supplied with sufficient phase precision by constituting the phase adjustment device of a clock signal using these variable delay circuits.

[Translation done.]